

AMENDMENTS TO THE CLAIMS:

1. (Previously presented) The semiconductor device according to claim 30, wherein said specified region comprises a circuit formation portion.
- 2-4. (Canceled)
5. (Currently amended) The semiconductor device according to claim ~~36~~ 30:
wherein one or more slit-like notches are formed at specified positions in said seal rings in such a manner that the respective slit-like notches in any two of said seal rings that are adjacent to each other are not aligned.
6. (Previously presented) The semiconductor device according to claim ~~36~~ 30, wherein, said at least one seal ring comprises a damascene wiring structure.
7. (Original) The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a single damascene wiring structure.
8. (Original) The semiconductor device according to claim 6, wherein said damascene wiring structure comprises a dual damascene wiring structure.
9. (Original) The semiconductor device according to claim 6, wherein said damascene

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wiring structure comprises a combination of a single damascene wiring structure and a dual damascene wiring structure.

10. (Canceled)

11. (Currently amended) The semiconductor device according to claim-~~36~~ 30, wherein:
said-at least one of said seal ring-rings is connected via a contact to a diffusion region formed in said semiconductor substrate, and
said contact and said diffusion region are formed so as to match approximately said at least one of said seal ring-rings in shape.

12. (Currently amended) The semiconductor device according to claim-~~36~~ 30, wherein:
said-at least one of said seal ring-rings is connected via a contact to a diffusion region formed in said semiconductor substrate, and
said contact and said diffusion region are formed without matching said at least one of said seal ring-rings in shape.

13. (Currently amended) The semiconductor device according to claim-~~36~~ 30, wherein
each of said at least one conductive layer-layers comprises copper or a copper-based conductive material.

14-29. (Canceled)

30. (Currently amended) A semiconductor device comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein ~~one or more~~ at least two wiring trenches are formed ~~in each of upwardly or downwardly through~~ said plurality of wiring insulating films along a periphery of said semiconductor chip in such a manner as to surround a specified region on said semiconductor substrate, said at least two wiring trenches including an outer wiring trench surrounding an inner wiring trench,

wherein in each of said ~~one or more~~ wiring trenches, a seal ring is formed by a conductive layer ~~is buried via a first conductive layer diffusion preventing film, in such a manner that the respective wiring trenches corresponding to each other in said plurality of wiring insulating films are connected with each other upwardly or downwardly, each seal ring being connected to a diffusion region formed in said semiconductor substrate,~~

wherein ~~each~~ at least one of said wiring ~~insulation film~~ insulating films comprises a low dielectric constant film comprising methyl-silsesquioxane or hydrogen-silsesquioxane, and a

wherein at least one second conductive layer diffusion preventing film is formed between a lower one and an upper one of said wiring insulating films, each second conductive layer diffusion preventing film being connected with a corresponding one of said first conductive layer diffusion preventing ~~films. films; and~~

~~wherein at least one of said wiring insulation films comprises a low dielectric constant film comprising methyl-silsesquioxane or hydrogen-silsesquioxane.~~

31-34. (Canceled)

35. (Currently amended) The semiconductor device according to claim ~~2~~ 30, wherein said diffusion region comprises an N-type diffusion region.

36. (Canceled)

37. (Currently amended) A a-semiconductor device, comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality of wiring insulating films stacked on top of each other in layers on a semiconductor substrate, and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein ~~one or more~~ at least two wiring trenches are formed ~~in each of~~ upwardly or downwardly through said plurality of wiring insulating films along a periphery of said semiconductor chip in such a manner as to surround a specified region on said semiconductor substrate, said at least two wiring trenches including an outer wiring trench surrounding an inner wiring trench,

wherein in each wiring trench, a seal ring is formed by a conductive layer is buried via a first conductive layer diffusion preventing film, ~~in such a manner that the respective wiring trenches corresponding to each other in said plurality of wiring insulating films are connected~~

~~with each other upwardly or downwardly, each seal ring being connected to a diffusion region~~
formed in said semiconductor substrate,

wherein ~~each~~ at least one of said wiring insulating ~~film-films~~ comprises a low
dielectric constant film having a dielectric constant lower than or equal to that of methyl-
silsesquioxane, and a

wherein at least one second conductive layer diffusion preventing film is formed
between a lower one and an upper one of said wiring insulating films, each second conductive
layer diffusion preventing film being connected with a corresponding one of said first
conductive layer diffusion preventing films. ~~films,~~ and

~~wherein at least one wiring insulating film comprises a low dielectric constant film~~
~~having a dielectric constant lower than or equal to that of methyl-silsesquioxane.~~

38. (Currently amended) A ~~a~~-semiconductor device, comprising:

a semiconductor chip provided with a circuit formation portion comprising a plurality
of wiring insulating films stacked on top of each other in layers on a semiconductor substrate,
and a multi-layer interconnection formed in said plurality of wiring insulating films,

wherein ~~one or more~~ at least two wiring trenches are formed ~~in each of~~ upwardly or
downwardly through said plurality of wiring insulating films along a periphery of said
semiconductor chip in such a manner as to surround a specified region on said semiconductor
substrate, said at least two wiring trenches including an outer wiring trench surrounding an
inner wiring trench,

wherein in each of said wiring-trench ~~trenches,~~ a seal ring is formed by a conductive

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layer is buried via a first conductive layer diffusion preventing film, ~~in such a manner that the~~
~~respective wiring trenches corresponding to each other in said plurality of wiring insulating~~
~~films are connected with each other upwardly or downwardly, each seal ring being connected~~
to a diffusion region formed in said semiconductor substrate,

wherein ~~each~~ at least one of said wiring insulating ~~film~~ films comprises a low
dielectric constant film having a dielectric constant lower than or equal to that of hydrogen-
silsesquioxane, and a

wherein at least one second conductive layer diffusion preventing film is formed
between a lower one and an upper one of said wiring insulating films and is connected with a
corresponding ~~one~~ ones of said first conductive layer diffusion preventing films. ~~films,~~ and

~~wherein at least one wiring insulating film comprises a low dielectric constant film~~
~~having a dielectric constant lower than or equal to that of hydrogen-silsesquioxane.~~